Attorney Docket No. LGHT 1054-0

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (withdrawn) An integrated circuit, comprising:

an array of function blocks, wherein each function block has an input and an output;

a predesigned routing structure formed over the array, including:

a plurality of vertical tracks,

wherein, in a first conducting layer of the predesigned routing structure, each track includes a pin in communication with a respective input or output and

wherein, in the first conducting layer, each track further includes a first vertical conductor, uncoupled to the pin.

2. (withdrawn) The integrated circuit of claim 1, wherein a second vertical conductor is formed in a second conducting layer, wherein the second vertical conductor is coupled to the first vertical conductor, but is uncoupled to the pin.

3. (withdrawn) The integrated circuit of claim 2, wherein the second vertical conductor is formed substantially under the pin.

4. (withdrawn) The integrated circuit of claim 1, further including a plurality of horizontal conductors that are formed under the first vertical conductors.

5. (withdrawn) The integrated circuit of claim 1, further including a customized conducting layer, wherein some conductors in the customized conducting layer are coupled to respective pins in the first conducting layer and other conductors in the customized conducting layer are coupled to respective first vertical conductors.

6. (withdrawn) The integrated circuit of claim 1, further including:

a customized conducting layer formed over the predesigned routing structure, wherein a first portion of the customized conducting layer formed over the pins is for local routing and a second portion of the customized conducting layer is for global routing.

7. (withdrawn) The integrated circuit of claim 1, further including:

a customized conducting layer formed over the predesigned routing structure and including a power line and a ground line.

8. (withdrawn) The integrated circuit of claim 1, wherein the predesigned routing structure is independent of any channels and is formed over each of the function blocks, wherein each function block remains usable.

9. (withdrawn) The integrated circuit of claim 1, further including:

a plurality of conductors for carrying at least one clock signal,

wherein the plurality of conductors are uncoupled to the pins or vertical conductors, and

wherein the plurality of conductors can be coupled with a custom conducting layer to form multiple independent clock domains.

10. (previously presented) An integrated circuit, comprising:

an array of function blocks, wherein each function block has an input and an output;

a predesigned routing structure formed over the array,

wherein the predesigned routing structure includes a plurality of conducting layers that include a plurality of conductive pin segments and a plurality of electrically unbroken conductive paths,

wherein each conductive pin segment carries a respective input or output,

wherein the structure includes a plurality of tracks, and

wherein in each track is located at least a portion of at least one respective electrically unbroken conductive path and at least one respective conductive pin segment in one of the plurality of conducting layers, and wherein the electrically unbroken conductive path is within the predesigned routing structure, ohmically unconnected to the respective conductive pin segment.

11. (previously presented) The integrated circuit of claim 10, wherein each electrically unbroken conductive includes portions formed on two conducting layers.

12. (previously presented) The integrated circuit of claim 10, wherein each electrically unbroken conductive includes portions formed on two conducting layers and wherein a portion of each electrically unbroken conductive path is formed substantially under the conductive pin segment located in the same track as the electrically unbroken conductive path.

13. (previously presented) The integrated circuit of claim 10, further including a customized conducting layer, wherein the customized conducting layer electrically connects first selected conductive pin segments to selected electrically unbroken conductive paths, second selected conductive pin segments to other selected conductive pin segments, third selected conductive pin segments to a power line, and fourth selected conductive pin segments to a ground line.

14. (previously presented) The integrated circuit of claim 10, further including:

a customized conducting layer formed over the predesigned routing structure and including a power line and a ground line, wherein the power line and the ground line are placed so as not to prevent the electrical connection of an electrically unbroken conductive path to a conductive pin segment by the customized conducting layer.

15. (previously presented) The integrated circuit of claim 10, further including:

a customized conducting layer formed over the predesigned routing structure, wherein a first portion of the customized conducting layer formed over the conductive pin segments is for local routing and a second portion of the customized conducting layer is for global routing.

16. (previously presented) The integrated circuit of claim 10, further including:

a plurality of conductors for carrying at least one clock signal, wherein the plurality of conductors are within the predesigned routing structure, ohmically unconnected to the conductive pin segments or electrically unbroken conductive paths, and wherein the plurality of conductors can be electrically interconnected in a custom conducting layer to form multiple clock domains.

17. (previously presented) An integrated circuit, comprising:

an array of function blocks, wherein each function block has an input and an output;

a predesigned routing structure formed over the array, including:

a first conducting layer having a plurality of parallel vertical tracks, wherein included in each track is a conductive pin segment carrying a respective input or output and in each track is a first portion of an electrically unbroken conductive path, wherein the conductive pin segment and the first portion are within the predesigned routing structure, ohmically unconnected to one another;

for each track, a second portion of the electrically unbroken conductive path, wherein the second portion is formed in at least one other conducting layer.

18. (previously presented) The integrated circuit of claim 17, wherein the second portion is formed substantially under the conductive pin segment for the respective track.

19. (previously presented) The integrated circuit of claim 17, wherein the electrically unbroken conductive path runs the vertical height of a function block.

20. (previously presented) The integrated circuit of claim 17, wherein the electrically unbroken conductive path is longer than the conductive pin segment.

21. (previously presented) The integrated circuit of claim 17, wherein for every other track in the first conducting layer, the second portion of the electrically unbroken conductive path is formed in a second conducting layer under the first conducting layer, for the remaining tracks, the second portion of the electrically unbroken conductive path is formed in a third conducting layer under the second conducting layer.

22. (previously presented) The integrated circuit of claim 17, wherein:

the predesigned routing structure further includes horizontal conductors formed under the first portion of the electrically unbroken conductive paths and connected through at least one via to the first conducting layer.

23. (previously presented) The integrated circuit of claim 17, further including a customized conducting layer wherein the customized conducting layer includes conductors that are connected through at least one via to the first conducting layer and wherein the customized conducting layer is used to form a user-defined circuit on the integrated circuit.

24. (previously presented) The integrated circuit of claim 17, further including a customized conducting layer formed over the predesigned routing structure, wherein a first portion of the customized conducting layer formed over the conductive pin segments is for local routing and a second portion of the customized conducting layer is for global routing.

25. (previously presented) The integrated circuit of claim 17, further including:

a customized conducting layer formed over the predesigned routing structure and including a power line and a ground line, wherein the power line and the ground line are placed so as not to prevent any desired electrical connection of an electrically unbroken conductive path to a conductive pin segment by the customized conducting layer.

26. (previously presented) The integrated circuit of claim 17, including:

a plurality of conductors for carrying at least one clock signal, wherein the plurality of conductors are within the predesigned routing structure, ohmically unconnected to the conductive pin segments or vertical conductors, and wherein the plurality of conductors can be electrically interconnected in a custom conducting layer to form multiple clock domains.

27. (previously presented) An integrated circuit, comprising:

an array of function blocks, to be used in the formation of a user-defined circuit, wherein each function block includes a device layer and at least one device interconnect layer, and wherein each function block has an input and an output;

a routing structure formed over the array including four conducting layers, the routing structure including:

a first predesigned conducting layer including a plurality of parallel vertical tracks, wherein each track includes a conductive pin segment carrying a respective input or output, and wherein each track includes a first portion of an electrically unbroken conductive path, wherein the conductive pin segment and the first portion of the electrically unbroken conductive path are ohmically unconnected to one another; in the first predesigned conducting layer,

a second predesigned conducting layer formed under the first conducting layer, wherein for a first group of alternate vertical tracks in the first conducting layer, the second conducting layer includes a second portion of each electrically unbroken conductive path, wherein the second portion is formed substantially under the respective conductive pin segment,

a third predesigned conducting layer formed under the second conducting layer, wherein for a second group of alternate vertical tracks in the first conducting layer, the third conducting layer includes a second portion of each electrically unbroken conductive

path, wherein the second portion is formed substantially under the respective conductive pin segment, and

a customized conducting layer formed over the first predesigned conducting layer and connected through at least one via to the first conducting layer, wherein the customized conducting layer has been formed in accordance with a user-defined circuit.

28. (previously presented) The integrated circuit of claim 27, wherein:

the second predesigned conducting layer includes horizontal conductors connected through at least one via to the first conducting layer.

29. (previously presented) The integrated circuit of claim 27, wherein the customized conducting layer includes a power line and a ground line, wherein the power line and the ground line are placed so as not to prevent any desired electrical connection of an electrically unbroken conductive path to a conductive pin segment by the customized conducting layer.

30. (original) The integrated circuit of claim 27, wherein:

the customized conducting layer has been formed into a local routing portion and a global routing portion.

31. (previously presented) The integrated circuit of claim 30, wherein:

the local routing portion is formed over the area occupied by theconductive pin segments of the first conducting layer.

32. (original) The integrated circuit of claim 27, wherein:

the second predesigned conducting layer includes conductors for use in clock distribution.

33. (previously presented) The integrated circuit of claim 27, wherein:

the second predesigned conducting layer includes conductors for use in clock distribution wherein the conductors for use in clock distribution can be electrically interconnected by a customized conducting layer to form multiple clock domains.

34. (currently amended) An integrated circuit, comprising:

an array of function blocks, wherein each function block has an input and an output;

a predesigned routing structure formed over the array, wherein the routing structure includes ~~a plurality of~~ four clock conductors~~, wherein the clock conductors~~ which can be electrically interconnected in a custom layer to form multiple clock domains, wherein a first one of the clock conductor extends vertically upwards, a second one of the clock conductor extends vertically downwards, a third one of the clock conductor extends horizontally to the right, and a fourth one of the clock conductor extends horizontally to the left.

35. (canceled)

36. (previously presented) The integrated circuit of ~~claim 35~~ claim 34, further including the custom layer, wherein the four clock conductors in a first function block are electrically interconnected to form a first clock tree, and wherein the four clock conductors in a second function clock are electrically interconnected to form a second clock tree.

37. (previously presented) An integrated circuit, comprising:

an array of function blocks, wherein each function block has an input and an output;

a predesigned routing structure formed over the array, including:

a first conducting layer having a plurality of parallel vertical tracks, wherein included in each track is a conductive pin segment carrying a respective input or output and in each track is a first portion of an electrically unbroken conductive path, wherein the conductive pin segment and the first portion are within the first conducting layer, ohmically unconnected to one another;

for each track, a second portion of the electrically unbroken conductive path, wherein the second portion is formed in at least one other conducting layer;

a plurality of clock conductors, wherein selected ones of the clock conductors can be electrically interconnected with a customized conducting layer to form multiple clock domains.

38. (previously presented) The integrated circuit of claim 37, wherein the second portion is formed substantially under the conductive pin segment for the respective track.

39. (previously presented) The integrated circuit of claim 37, wherein the electrically unbroken conductive path runs the vertical height of a function block.

40. (previously presented) The integrated circuit of claim 37, wherein the electrically unbroken conductive path is longer than the conductive pin segment.

41. (previoulsy presented) The integrated circuit of claim 37, wherein for every other track in the first conducting layer, the second portion of the electrically unbroken conductive path is formed in a second conducting layer under the first conducting layer, and wherein for the remaining tracks, the second portion of the electrically unbroken conductive path is formed in a third conducting layer under the second conducting layer; and

wherein the plurality of clock conductors are formed in the second conducting layer.

42. (previously presented) The integrated circuit of claim 37, further including the customized conducting layer, wherein the customized conducting layer includes conductors that are connected through at least one via to the first conducting layer and wherein the customized conducting layer is used to form a user-defined circuit on the integrated circuit.

43. (previously presented) The integrated circuit of claim 37, wherein the plurality of clock conductors includes four clock conductors in a second conducting layer formed under the

first conducting layer, wherein the four conductors are ohmically unconnected to one another in the second conducting layer.